Professional Course (Odd) Examination, 2025

(3rd Semester)

BACHELOR OF COMPUTER APPLICATIONS

(Computer Organization and Architecture)

Full Marks : 75

Time : 3 hours

The figures in the margin indicate full marks for the questions

(PART : A—OBJECTIVE)

(*Marks* : 25)

SECTION—I

(*Marks* : 15)

I. Tick (✓) the correct answer in the brackets provided : 1×10=10

1. What does the '←' symbol represent in Register Transfer Language (RTL)?

   (a) Logical AND ( ) *(b)* Memory write ( )

   (c) Data transfer ( ) *(d)* Control signal ( )

2. A shift micro-operation can be used to

   (a) multiply or divide by 2 ( )

   (b) add two registers ( )

   (c) decode instructions ( )

   (d) load data from memory ( )

3. The register that holds the address of the next instruction is
   (a) stack pointer ( )
   (b) instruction register ( )
   (c) program counter ( )
   (d) memory data register ( )

4. Which register has only 12 numbers of bits?
   (a) TR ( ) (b) INPR ( )
   (c) DR ( ) (d) AR ( )

5. The number of general purpose registers is typically higher in
   (a) RISC ( )
   (b) CISC ( )
   (c) stack-based CPUs ( )
   (d) None of the above ( )

6. In stack organization, the POP operation
   (a) adds an item ( )
   (b) removes the top item ( )
   (c) loads memory ( )
   (d) shifts data ( )

7. Which I/O mode is most efficient for transferring large blocks of data?
   (a) Programmed I/O ( )
   (b) Polling ( )
   (c) Interrupt-Driven I/O ( )
   (d) DMA ( )

8. Which component is responsible for initiating Interrupt-Driven I/O?
   (a) CPU ( ) (b) I/O device ( )
   (c) Memory ( ) (d) ALU ( )

9. Which memory connection type is used for auxiliary storage?
   (a) RAM ( ) (b) Cache ( )
   (c) Magnetic Disk ( ) (d) ROM ( )

10. In associative mapping, how is data located in the cache?

(a) By direct address ( )

(b) By content matching ( )

(c) By page number ( )

(d) By memory block ( )

II. State whether the following statements are *True (T)* or *False (F)* by putting a Tick (✓) mark in the brackets provided : 1×5=5

1. Shift micro-operations are not parts of Register Transfer Language (RTL).

(T / F)

2. The Program Counter (PC) is updated after the execute phase of the instruction cycle.

(T / F)

3. Register stack instructions include memory stack operations.

(T / F)

4. Isolated versus memory-mapped I/O includes an example of I/O interface.

(T / F)

5. Virtual memory does not involve address mapping.

(T / F)

SECTION—II

(*Marks* : 10)

III. Answer the following questions : 2×5=10

1. Define micro-operations.
2. Differentiate between Direct and Indirect addressing modes with an example.
3. What are one-address instructions? Give examples.
4. What are the main modes of transfer in DMA?
5. Define associative mapping in memory organization.

(PART : B—DESCRIPTIVE)

(*Marks* : 50)

IV. Answer the following questions : 10×5=50

1. Define register transfer. Design a 4-bit full adder with necessary diagram and truth table. 3+7=10

OR

What is a three-state buffer? Illustrate the working of a three-state buffer. 2+8=10

2. What are computer registers? Explain the different types of register briefly. 2+8=10

OR

Explain the instruction cycle of a computer system in detail with a neat diagram. Discuss each phase of the cycle highlighting the operations performed in each step. 5+5=10

3. Define instruction format. Explain the different types of instruction format with example. 2+8=10

OR

Describe the general stack organization in a CPU. Explain stack organization with examples of registers and memory stack. 5+5=10

4. Discuss programmed I/O, interrupt-initiated I/O and DMA. Compare their performances. 2+8=10

OR

Describe asynchronous data transfer and strobe control. Explain handshaking in I/O operations with detailed example. 4+6=10

5. Explain memory hierarchy and its significance. Describe the organization of RAM and ROM chips. 5+5=10

OR

What is auxiliary memory? Discuss the concept of cache memory and its mapping technique. 3+7=10

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