Professional Course Examination (Odd), 2023

(1st Semester)

BACHELOR OF COMPUTER APPLICATIONS

Course No. : BCA/1/CC/04

(Digital Computer Fundamentals)

Full Marks : 75

Time : 3 hours

The figures in the margin indicate full marks for the questions

(PART : A—OBJECTIVE)

(*Marks* : 25)

SECTION—A

(*Marks* : 15)

A. Tick (✓) the correct answer in the brackets provided : 1×10=10

1. BCD stands for
   (a) binary coded decimal ( )
   (b) binary common decimal ( )
   (c) basic carrier decimal ( )
   (d) based counter decimal ( )
2. The 10's complement of $(4136)_{10}$ is
   (a) 5841 ( )
   (b) 5864 ( )
   (c) 5844 ( )
   (d) 5874 ( )
3. A register is a group of _____ suitable for storing binary information.
   (a) counters ( ) *(b)* adders ( )
   (c) flip-flops ( ) *(d)* substractors ( )

4. What is the octal equivalent of the binary number 10111101?

(a) 675 ( ) *(b)* 275 ( )

(c) 572 ( ) *(d)* 573 ( )

5. Ripple counters are sometimes called

(a) synchronous counters ( )

(b) registers ( )

(c) asynchronous counters ( )

(d) program counters ( )

6. The master-slave *J-K* flip-flop is effectively a combination of

(a) an SR flip-flop and a T flip-flop ( )

(b) an SR flip-flop and a D flip-flop ( )

(c) a T flip-flop and a D flip-flop ( )

(d) two T flip-flops ( )

7. The output of half adder is in the form of

(a) sum ( )

(b) carry ( )

(c) sum and carry ( )

(d) None of the above ( )

8. How many cells are there in an *n*-variable K-map?

(a) $2n$ ( ) *(b)* $2n \quad a$ ( )

(c) $2n \quad a$ ( ) *(d)* n^2 ( )

9. The D flip-flop is a modification of

(a) JK flip-flop ( ) *(b)* T flip-flop ( )

(c) RS flip-flop ( ) *(d)* clocked RS flip-flop ( )

10. SR-type flip-flop can be converted into D flip-flop, if S is connected to R through

(a) EX-OR gate ( ) *(b)* inverters ( )

(c) AND gate ( ) *(d)* full adder ( )

B. State whether the following statements are *True (T)* or *False (F)* by putting a Tick (✓) mark : 1×5=5

1. The other name of D flip-flop is delay flip-flop.

(T / F)

2. Decoders are used for converting one type of number system into the other form.

(T / F)

3. NAND gate is known as universal gate.

(T / F)

4. Parallel counter is also called shift counter.

(T / F)

5. Boolean algebra obeys distributive law and commutative law.

(T / F)

SECTION—II

(*Marks* : 10)

C. Answer the following questions : 2×5=10

1. *(a)* What is arithmetic shift?

OR

(b) What is flip-flop?

2. *(a)* Construct full adder.

OR

(b) Construct half adder.

3. *(a)* Simplify $y \quad (\overline{A} \quad B)(A \quad B)$

OR

(b) What is error detection code?

4. *(a)* Construct 2 : 1 multiplexer.

OR

(b) Construct 1 : 4 demultiplexer.

5. *(a)* What are alphanumeric codes?

OR

(b) What is combinational circuit?

(PART : B—DESCRIPTIVE)

(*Marks* : 50)

1. *(a)* Convert the $(11010101011)_2$ into octal, hexadecimal, decimal number system. 6

(b) Convert the $(5.A08C)_{16}$ into octal and binary number system. 4

OR

(c) Explain digital computer system with the help of diagram. 5

(d) Simplify the following : 5

(i) $\overline{A}\ \overline{B}\ \overline{C} \quad \overline{A}\ B\ \overline{C}$

(ii) $\overline{ABC} \quad \overline{A}B\overline{C} \quad A\overline{BC} \quad AB\overline{C}$

2. *(a)* Simplify the Boolean expression using K-map : 6

$F(A, B, C, D, E) \qquad m(0, 1, 4, 5, 16, 1721, 25, 29)$

(b) Express the Boolean function $F \quad xy \quad x\,z$ as a product of maxterms. 4

OR

(c) Explain two, three and four variable K-maps. 6

(d) Using De Morgan's theorem, prove $(A \quad B) \quad A \quad B$. 4

3. *(a)* Give the logic symbol and truth table of the following logic gates : 6

(i) OR

(ii) NAND

(iii) XOR

(b) Subtract a binary number (1010) from (1111) using 2's complement method. 4

OR

(c) Implement a Boolean function $F \quad \overline{AB} \quad ABC \quad (\overline{B \quad C})$ using logic gates. 5

(c) Divide the binary number 110111 by 101. 5

4. *(a)* What is multiplexer? Discuss the working of 4 : 1 multiplexer with logic circuit and truth table. 6

(b) Write a short note on programmable logic array. 4

OR

(c) Explain the working of full adder with logic diagram, logic circuit and truth table. 6

(d) Design a 2- to 4-decoder. Show the truth table with logic diagram. 4

5. *(a)* What is shift register? Explain serial input shift register and parallel input shift register. 6

(b) Explain master-slave flip-flop with a suitable logic diagram. 4

OR

(c) Explain four-bit ripple counter with a timing diagram. 6

(d) Differentiate between synchronous counter and asynchronous counter. 4

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